IN THE SPECIFICATION

Please amend the title of the invention as follows:

METHOD OF MANUFACTURING A DUAL GATE SEMICONDUCTOR DEVICE ~~AND METHOD OF MANUFACTURE THEREOF~~ WITH A POLY-METAL ELECTRODE

Please insert the following subheading and paragraph on page 1, following the title:

--CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of application Serial No. 09/639,306 filed on August 16, 2000, now U.S. Patent No. 6,503,788. This application is related to application Serial No. 10/272,369 filed on October 17, 2002, now U.S. Patent No. 6,645,799, which is a divisional of application Serial No. 09/639,306 filed on August 16, 2000, now U.S. Patent No. 6,503,788, and application Serial No. 10/448,351 filed May 30, 2003, which is a divisional of application Serial No. 09/639,306 filed on August 16, 2000, now U.S. Patent No. 6,503,788. The contents of application Serial Nos. 09/639,306, 10/272,369 and 10/448,351 are hereby incorporated herein by reference in their entirety.--

Please replace the paragraph on page 1, lines 2-5, with the following amended paragraph:

The present invention relates to a CMOS (Complementary Metal-oxide Semiconductor) type semiconductor device having [[as]]a gate electrode of p type and n type conductive polycrystalline silicon and a method of manufacture thereof.

Please replace the paragraph beginning at page 9, line 23, with the following rewritten paragraph:

Next, for forming a p-type well area 3 and an n-type well area 4 at a predetermined areas where a p-channel and an n-channel MOS transistors are to be formed, boron is ion-implanted into the left-half portion and phosphorus is ion-implanted into the right-half portion. Then, the annealing of 1000°C in a nitrogen atmosphere is carried out for 20 minutes. Afterwards, by oxidizing the surface of the substrate at 850°C, an SiO_2 film having a thickness of 2.8 nm is formed. Then, the surface is heat-treated at an oxide nitrogen atmosphere for forming a silicon oxide nitride film (silicon oxynitride) 5. These annealings complete a gate insulating film 5 of 3 nm (see Fig. 3B). The impurity concentration on the surface of the substrate that is approximate to adjusting the threshold voltage of each MOS transistor may be achieved by ion-implanting phosphorus or boron in the range of $1 \times 10^{12}/cm^2$ to $3 \times 10^{13}/cm^2$. In addition, though various implantations are tried, even for the dual gate CMOS based on the conventional method, the manufacturing conditions of the MOS transistor having the most approximate threshold voltage are not defined.

Please replace the paragraph beginning at page 12, line 9, with the following rewritten paragraph:

Next, vapor is added to the hydrogen atmosphere at a pressure ratio of 10 % and then the annealing is performed at 750°C and for 30 minutes. This heat treatment results in oxidizing the silicon substrate surface 12 around the gate electrode and the side wall 13 of the gate electrode silicon layer under W/WNx that has been changed from an amorphous material into a polycrystalline material. In

addition, the annealing at the atmosphere of vapor-added hydrogen results in selectively oxidizing the exposed silicon surface without oxidizing the tungsten [[8]]10 and the tungsten nitride [[10]]9. This process for selectively oxidizing the silicon is intended to recovering reliability of the gate oxide film that was subject to damage in the dry-etching process. After the process of re-oxidizing the silicon substrate, a resist pattern for covering the PMOS area is formed by means of the normal photolithography technique. With the resist pattern and the silicon nitride film 11 on the NMOS area as mask materials, by using the ion-implanting device, phosphorus ions of $2 \times 10^{13}/cm^2$ are implanted onto the silicon substrate at 10 keV for forming an n-type semiconductor area 14. Then, the resist pattern for covering the NMOS area is formed by means of the normal photolithography technique. With this resist pattern and the silicon nitride film 11 of the pMOS area as the masks, BF2 ions of $2 \times 10^{14}/cm^2$ are implanted at 10 keV by means of the ion-implanting method, for forming a p-type semiconductor area 15 (see Fig. 4C).